IN THE CLAIMS

Kindly amend claim 1 as shown in the following claim listing:

1. (currently amended) A voltage limiting semiconductor pass gate circuit (15), comprising a first transistor (16, 21) being operatively connected between an input node (10) and an output node (11) of said pass gate circuit (15), the first transistor (16, 21) having a control electrode being biased to a supply voltage (6), characterized by the control electrode being biased to the supply voltage (6) by a resistor (12 connected in series with two back-to-back connected diode elements (18, 19).

2. (original) A semiconductor pass gate circuit (15) according to claim 1, wherein said diode elements (18, 19) are comprised of diode connected transistors.

3. (original) A semiconductor pass gate circuit (15) according to claim 1, wherein the semiconductor pass gate circuit (15) further comprises a second transistor (17) being operatively connected between said input node (10) and said output node (11), the second transistor (17) having a further control electrode coupled to the control electrode of the first transistor (16) via the two back-to-back connected diode elements (18, 19).

4.(original) An input I/O cell (14) for use with integrated semi-conductor circuits, said I/O cell (14) having an input terminal (2), an output terminal (3) and at least one level detector circuit (4) coupled between said input terminal (2) and said output terminal (3), characterized by a semiconductor pass

gate circuit (15) in accordance with claim 1, coupled between said input terminal (2) and said level detector circuit (4).

5.(original) An input I/O cell (14) according to claim 4, wherein said level detector circuit comprises a hysteresis circuit (4).

6. (original) An input I/O cell (14) according to claim 5, wherein said hysteresis circuit (4) is hysteresis inverter circuit.

7. (original) An input I/O cell (14) according to claim 6, wherein a further inverter circuit (5) couples said hysteresis inverter circuit (4) to said output terminal (3).

8. (original) An integrated circuit (13) compromising at least one input I/O cell (14) in accordance with claim 4.